09/394,302

1-54. (Cancelled)

55. (Currently Amended) A transportable integrated circuit chip test device comprising:

a transportable test box adapted to surround integrated circuit chips during transportation of said integrated circuit chips;

a plurality of test boards mounted in said test box adapted to test said integrated circuit chips while in-transit; and

a portable power supply in said test box connected to said test boards adapted to supply power to said test boards while in-transit,

wherein each of said test boards comprises:

sockets adapted to hold integrated circuit chips ~~to be tested while being transported~~; and

testing circuitry electrically connected to said sockets.

56. (Previously Presented) The device in claim 55, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

57. (Previously Presented) The device in claim 55, wherein said portable power supply comprises a battery.

58. (Previously Presented) The device in claim 55, wherein each of said test boards includes a memory adapted to store test results.

59. (Previously Presented) The device in claim 55, wherein each of said test boards includes a known good integrated circuit chip.

60. (Previously Presented) The device in claim 59, wherein each of said test boards includes comparators electrically connected to said sockets.

61. (Previously Presented) The device in claim 60, wherein said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip, and

wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips.

62. (Previously Presented) The device in claim 61, wherein said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously.

63. (Currently Amended) A transportable integrated circuit chip test device adapted to test application specific integrated circuit (ASIC) chips, said device comprising:

a transportable test box adapted to surround integrated circuit chips during transportation of said integrated circuit chips;

a plurality of test boards mounted in said test box adapted to test said integrated circuit chips while in-transit; and

a portable power supply in said test box connected to said test boards adapted to supply power to said test boards while in-transit,

wherein each of said test boards comprises:

sockets adapted to hold ASIC chips ~~to be tested while being transported~~; and

testing circuitry electrically connected to said sockets, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said ASIC chips simultaneously, and

wherein said testing circuitry identifies a defective ASIC chip as one having a different output when compared to outputs of the other ASIC chips, when all ASIC chips are supplied with identical inputs.

64. (Previously Presented) The device in claim, 63 wherein all of said ASIC chips have an identical design.

65. (Previously Presented) The device in claim 63, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

66. (Previously Presented) The device in claim 63, wherein said portable power supply comprises a battery.

67. (Previously Presented) The device in claim 63, wherein each of said test boards includes a memory adapted to store test results.

68. (Previously Presented) The device in claim 63, wherein each of said test boards includes a known good integrated circuit chip.

69. (Previously Presented) The device in claim 68, wherein all of said comparators are connected to said known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip.

70. (Previously Presented) The device in claim 63, wherein by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested.

71-96 (Cancelled).

97. (New) A method for testing integrated circuit chips comprising:
transporting said integrated circuit chips; and
testing said integrated circuit chips during said transporting.

98. (New) The method in claim 97, further comprising supplying power to a test circuit connected to said integrated circuit chips during said transporting.

99. (New) The method in claim 97, further comprising identifying ones of said integrated circuit chips which failed said testing.

100. (New)The method in claim 99, wherein said identifying comprises storing results of said testing in a memory.

101. (New)The method in claim 99, wherein said identifying comprises displaying a visual indicator of passing or failing chips

102. (New)The method in claim 99, wherein said testing includes comparing output signals of said integrated circuit chips with each other.

103. (New)The method in claim 97, wherein said testing includes comparing output signals of one integrated circuit chip with output signals of all other integrated circuit chips that have not been identified as defective.

104. (New)The method in claim 97, wherein said testing includes comparing output signals of said integrated circuit chips with a golden chip.